CLAIMS

What is claimed is:

1. A method of manufacturing a thin film transistor (TFT), comprising:

forming a semiconductor layer over a substrate using a first mask;

forming a first insulating layer over a whole surface of the substrate;

forming a gate electrode having a capping layer over the first insulating layer using a second mask;

forming spacers on both side wall portions of the gate electrode and the capping layer over the first insulating layer while exposing both end portions of the semiconductor layer;

forming high-density source and drain regions by ion-implanting a high-density impurity to the exposed portions of the semiconductor layer; and

forming source and drain electrodes without contact holes in the first insulating layer, using a third mask which directly contact the high-density source and drain regions.

2. The method of claim 1, wherein said forming of the spacers comprises:

depositing a second insulating layer over the whole surface of the substrate; and

patterning the second insulating layer and the first insulating layer to form the spacers so as to expose both the end portions of the semiconductor layer.

3. The method of claim 2, wherein the second insulating layer, the first insulating layer, and the capping layer are made of one of an oxide layer and a nitride layer.

4. The method of claim 1, further comprising forming low-density source and drain regions by ion-implanting a low-density impurity having a same conductivity type as the high-density impurity to the semiconductor layer after said forming of the gate electrode, so as to have the semiconductor layer with lightly doped drain (LDD) regions formed under the spacers.

5. The method of claim 1, further comprising forming a silicide layer to exposed portions of the high-density source and drain regions of the semiconductor layer.

6. The method of claim 5, wherein the forming of the silicide layer comprises:

forming a second metal layer over the whole surface of the substrate having the

semiconductor layer, the first insulating layer, the gate electrode and the spacers; and

using a silicide process to form the silicide layer.

7. The method of claim 6, wherein the second metal layer for forming the silicide layer is made of a refractory metal, and the first insulating layer, the capping layer, the third insulating layer, and the buffer layer are one of an oxide layer and a nitride layer.

8. The method of claim 1, further comprising forming a silicide layer to the exposed portions of the semiconductor layer after said forming of the spacers.

9. The method of claim 8, wherein the forming of the high-density source and drain regions comprises using the silicide layer to minimize harm to the semiconductor layer during an ion-implanting process of the high-density impurity.

10. The method of claim 1, wherein said forming of the source and drain electrodes without the contact holes comprises:

forming a third metal layer over the whole surface of the substrate having the semiconductor layer, the first insulating layer, the gate electrode and spacers; and

patterning the third metal layer using the third mask to form the source and drain electrodes without the contact holes in the first insulating layer.

11. An active matrix display device manufactured by the method of claim 1.

12. A thin film transistor (TFT), comprising:

a substrate;

a semiconductor layer formed over said substrate having end portions;

a first insulating layer disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer;

a gate electrode formed over said first insulating layer;

a capping layer formed over said gate electrode;

spacers formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer;

high-density source and drain regions formed at the ones of the end portions of said

semiconductor layer exposed beyond said spacers; and

source and drain electrodes which directly contact, respectively, said high density source and drain regions.

13. The TFT of claim 12, further comprising low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at regions of said semiconductor layer under said spacers, wherein said semiconductor layer has lightly doped drain (LDD) regions under said spacers.

14. The TFT of claim 12, wherein said first insulating layer, said capping layer and said spacer are one of an oxide layer and a nitride layer.

15. The TFT of claim 12, further comprising a silicide layer formed between said source electrode and said high-density source region and between said drain electrode and said high-density drain region.

16. The TFT of claim 15, wherein said silicide layer is of a refractory metal.

17. A method of manufacturing an active matrix display device, comprising:

forming a semiconductor layer having end portions over a substrate using a first mask;

forming a first insulating layer over a whole surface of the substrate;

forming a gate electrode having a capping layer over the first insulating layer using a second mask;

forming spacers on both side wall portions of the gate electrode and the capping layer over the first insulating layer to expose ones of the end portions of the semiconductor layer;

forming high-density source and drain regions by ion-implanting a high-density impurity to the exposed portions of the semiconductor layer;

forming source and drain electrodes without contact holes in the first insulating layer, using a third mask to directly contact the high-density source and drain regions, respectively;

forming a second insulating layer over the whole surface of the substrate;

forming an opening portion by etching the second insulating layer using a fourth mask and exposing a portion of one of the source and drain electrodes; and

forming a pixel electrode on the second insulating layer, the pixel electrode contacting

the exposed electrode of the source and drain electrodes.

18. The method of claim 17, further comprising forming low-density source and drain regions by ion-implanting a low-density impurity having a same conductivity type as the high-density impurity to the semiconductor layer after said forming of the gate electrode so as to have the semiconductor layer with lightly doped drain (LDD) regions formed under the spacers.

19. The method of claim 17, further comprising forming a silicide layer at the exposed portions of the semiconductor layer after said forming of the spacers.

20. The method of claim 17, further comprising sequentially forming an organic electro-luminescence (EL) layer and a cathode electrode on a first predetermined area of the pixel electrode and on a second predetermined area of the second insulating layer.

21. An active matrix display device manufactured by the method of claim 17.

22. An active matrix display device, comprising:

a substrate;

a semiconductor layer having end portions formed over said substrate;

a first insulating layer formed over said semiconductor layer so as to expose one of the end portions of said semiconductor layer;

a gate electrode formed over said first insulating layer;

a capping layer formed over said gate electrode;

spacers formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer;

high-density source and drain regions formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers;

source and drain electrodes which directly contact, respectively, said high density source and drain regions;

a planarization layer having an opening portion which exposes a portion of one of said source and drain electrodes; and

a pixel electrode formed on the planarization layer, the pixel electrode contacting one of the second source and drain electrodes through the opening portion.

23. The active matrix display device of claim 22, further comprising low-density source and drain regions having a same conductivity as said high-density source and drain regions formed at off-set regions of said semiconductor layer under said spacers so as to have said semiconductor layer with lightly doped drain (LDD) regions under said spacers.

24. The active matrix display device of claim 22, further comprising silicide layers formed between said source electrode and said high-density source region and between said drain electrode and said high-density drain region.

25. The active matrix display device of claim 22, further comprising an organic electro-luminescence (EL) layer and a cathode electrode sequentially formed on a first predetermined area of said pixel electrode and on a second predetermined area of said planarization layer.